AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An apparatus ~~circuit~~ comprising:

a buffer for storing data~~, wherein the buffer includes a plurality of entries~~;

a write pointer coupled to the buffer, wherein the write pointer is configured to ~~sequentially indicate each one of the plurality of entries~~ point to an entry in the buffer into which data is to be written, ~~wherein~~ the write pointer ~~is~~ to be clocked by a first clock;

a read pointer coupled to the buffer, wherein the read pointer is configured to ~~sequentially indicate each one of said plurality of entries~~ point to an entry in the buffer from which data is to be read, ~~wherein~~ the read pointer ~~is~~ to be clocked by a second clock that has a same clock frequency as the first clock; and

a ~~first~~ circuit configured to ~~generate~~ transfer a pointer value of the write pointer as the read pointer in response to an indication that a predetermined pattern of data is transmitted to the buffer for storage~~, wherein the first circuit is coupled to the read pointer~~; and

a synchronizing circuit coupled to the ~~read pointer and~~ circuit to receive the indication~~, wherein the synchronizing circuit is configured to generate a signal to the read pointer responsive to the indication;~~

~~wherein said read pointer is configured to update to the pointer value from the first circuit responsive to the signal~~ of the predetermined pattern and, in response, to compensate for a skewing of the second clock from the first clock by synchronizing commencement of the read pointer to read from the buffer after data that is written into the buffer is stable.

2. (currently amended) The ~~circuit~~ apparatus as recited in claim 1 ~~wherein the pointer value is a write pointer value of the write pointer concurrent with the indication, and~~ wherein the circuit ~~is~~ includes a storage circuit configured to capture the ~~write~~ pointer value in response to the indication.

3. (currently amended) The ~~circuit~~ apparatus as recited in claim ~~1 further comprising a logic circuit coupled to the synchronizing circuit and configured to provide the indication~~ 2 wherein the circuit includes a latch to latch the pointer value.

4. (canceled)

5. (currently amended) The ~~circuit~~ apparatus as recited in claim ~~4~~ 1, wherein the synchronizing circuit further ~~comprises~~ includes a delay circuit ~~coupled to the synchronizer and configured to delay generation of the signal in response to the indication for~~ to introduce a predetermined delay to delay commencement of the read pointer after commencement of the write pointer.

6. (currently amended) The ~~circuit~~ apparatus as recited in claim 5, wherein the delay circuit is clocked by the second clock.

7. (currently amended) The ~~circuit~~ apparatus as recited in claim 6, wherein the delay circuit ~~comprises~~ includes a predetermined number of flip-flops.

8. (currently amended) The ~~circuit~~ apparatus as recited in claim 6, wherein the delay circuit ~~comprises~~ includes a configurable number of flip-flops.

9. (currently amended) The ~~circuit~~ apparatus as recited in claim 1, wherein the write pointer includes a ~~first~~ write counter ~~which generates a write counter~~ to change a write pointer value~~, wherein the write counter value addresses the buffer~~ to select subsequent entries in the buffer to write subsequent data.

10. (currently amended) The ~~circuit~~ apparatus as recited in claim 9, wherein the write counter is an ~~up~~ incremental counter.

11. (currently amended) The ~~circuit~~ as recited in claim ~~1~~ 10, wherein the read pointer includes a ~~second~~ read counter ~~which generates a read counter~~ to change a read pointer value, ~~wherein the read counter value addresses the buffer~~ to select subsequent entries in the buffer to read subsequent data.

12. (currently amended) The ~~circuit~~ apparatus as recited in claim 11, wherein the read counter is an ~~up~~ incremental counter.

13. (currently amended) The ~~circuit~~ apparatus as recited in claim 1, wherein the ~~first~~ circuit detects which ~~of the plurality of entries~~ entry or entries in the buffer is updated with the predetermined pattern of data ~~to generate the pointer value~~.

14. (currently amended) A method of initializing a buffer, ~~the method~~ comprising:

detecting a predetermined pattern of data transmitted for storage in ~~one of a plurality of entries~~ an entry in the buffer ~~responsive to a first clock~~;

generating a pointer value for a write pointer in response to the detecting the predetermined pattern of data to initialize writing of subsequent data;

transferring the pointer value of the write pointer to a read pointer to initialize the read pointer;

writing subsequent data into the buffer by changing the pointer value in the write pointer; and

synchronizing ~~an indication of the detecting to a second clock~~ the read pointer to commence reading from the buffer after a delay to compensate for a skewing of a first clock used to write data into the buffer and a second clock used to read data from the buffer, the second clock having a same frequency as the first clock;

~~updating a read pointer to said pointer value responsive to the synchronizing~~.

15. (currently amended) The method as recited in claim 14 wherein the synchronizing ~~comprises~~ includes delaying for a predetermined number of cycles of the second clock.

16. (canceled)

17. (currently amended) The method as recited in claim ~~16~~ 15, wherein the ~~generating the write~~ changing the pointer value in the write pointer includes incrementing a ~~first counter~~ count responsive to the ~~second~~ first clock.

18. (currently amended) The method as recited in claim ~~14~~ 17 further comprising ~~generating~~ changing a read pointer value used by the read pointer ~~to indicate each one of said plurality of entries in the buffer~~ by incrementing a count responsive to the second clock.

19-20. (canceled)

21. (currently amended) The method as recited in claim 14 wherein the generating a pointer value ~~comprises~~ includes detecting which ~~of the plurality of entries~~ entry or entries in the buffer is updated with the predetermined pattern of data.